

## General purpose JFET dual operational amplifiers

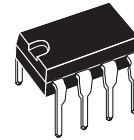
### Features

- Wide common-mode (up to  $V_{CC}^+$ ) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch up free operation
- High slew rate: 16 V/ $\mu$ s (typical)

### Description

The TL082, TL082A and TL082B are high speed JFET input dual operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

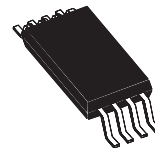
The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.



**N**  
**DIP8**  
(Plastic package)

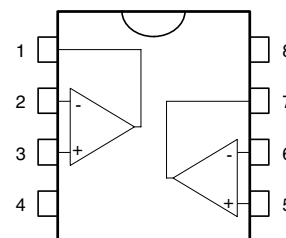


**D**  
**SO-8**  
(Plastic micropackage)



**P**  
**TSSOP8**  
(Thin shrink small outline package)

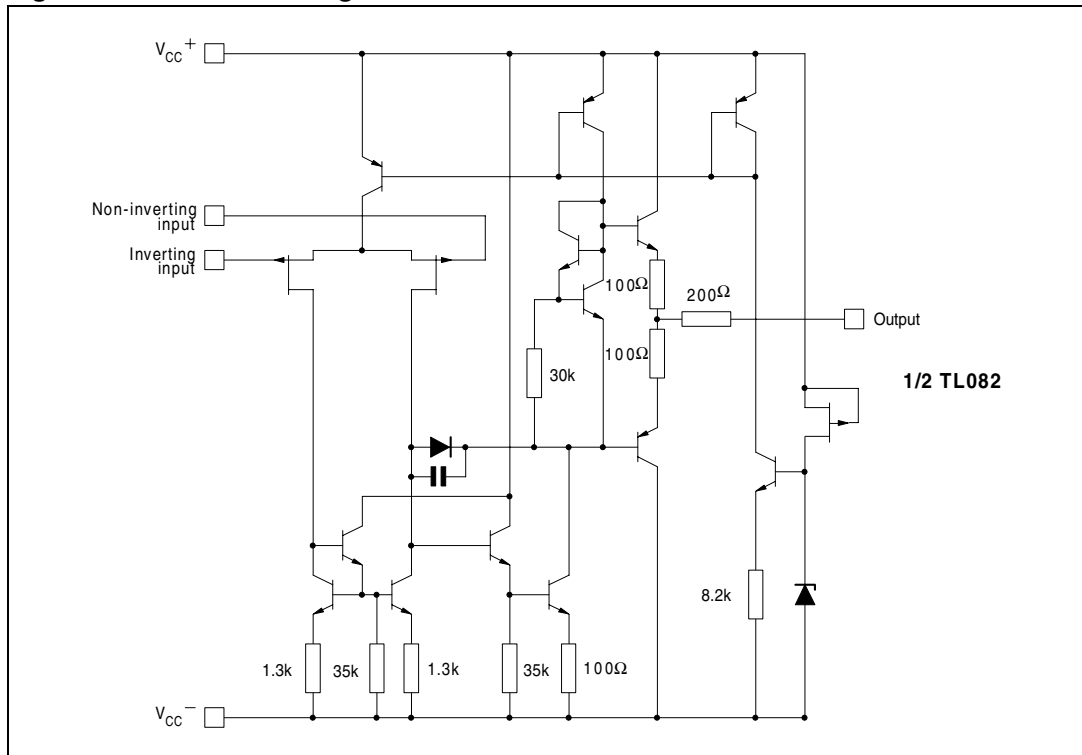
#### Pin connections (top view)



- 1 - Output 1
- 2 - Inverting input 1
- 3 - Non-inverting input 1
- 4 -  $V_{CC}^-$
- 5 - Non-inverting input 2
- 6 - Inverting input 2
- 7 - Output 2
- 8 -  $V_{CC}^+$

# 1 Schematic diagram

Figure 1. Schematic diagram



## 2 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings**

Symbol	Parameter	TL082I, AI, BI	TL082C, AC, BC	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	±18		V
$V_{in}$	Input voltage <sup>(2)</sup>	±15		V
$V_{id}$	Differential input voltage <sup>(3)</sup>	±30		V
$P_{tot}$	Power dissipation	680		mW
$R_{thja}$	Thermal resistance junction to ambient <sup>(4)</sup>			°C/W
	SO-8	125		
	DIP8	85		
	TSSOP8	120		
$R_{thjc}$	Thermal resistance junction to case			°C/W
	SO-8	40		
	DIP8	41		
	TSSOP8	37		
	Output short-circuit duration <sup>(5)</sup>	Infinite		
$T_{stg}$	Storage temperature range	-65 to +150		°C
ESD	HBM: human body model <sup>(6)</sup>	1		kV
	MM: machine model <sup>(7)</sup>	200		V
	CDM: charged device model <sup>(8)</sup>	1500		V

- All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between  $V_{CC}^+$  and  $V_{CC}^-$ .
- The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
- Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.
- The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
- Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

**Table 2. Operating conditions**

Symbol	Parameter	TL082I, AI, BI	TL082C, AC, BC	Unit
$V_{CC}$	Supply voltage	6 to 36		V
$T_{oper}$	Operating free-air temperature range	-40 to +105	0 to +70	°C

### 3 Electrical characteristics

Table 3.  $V_{CC} = \pm 15V$ ,  $T_{amb} = +25^{\circ}C$  (unless otherwise specified)

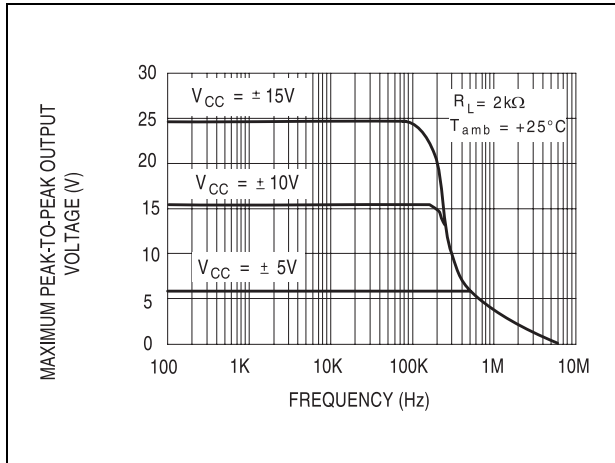
Symbol	Parameter	TL082I,AC,AI,BC, BI			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$V_{io}$	Input offset voltage ( $R_S = 50\Omega$ ) $T_{amb} = +25^{\circ}C$		3	10		3	10	mV
	TL082 TL082A TL082B		3 1	6 3				
	$T_{min} \leq T_{amb} \leq T_{max}$			13		13		
$DV_{io}$	Input offset voltage drift		10			10		$\mu V/^{\circ}C$
$I_{io}$	Input offset current <sup>(1)</sup> $T_{amb} = +25^{\circ}C$		5	100		5	100	pA nA
	$T_{min} \leq T_{amb} \leq T_{max}$			4		10		
$I_{ib}$	Input bias current $T_{amb} = +25^{\circ}C$		20	200		20	400	pA nA
	$T_{min} \leq T_{amb} \leq T_{max}$			20		20		
$A_{vd}$	Large signal voltage gain ( $R_L = 2k\Omega$ , $V_o = \pm 10V$ ) $T_{amb} = +25^{\circ}C$	50	200		25	200		V/mV
	$T_{min} \leq T_{amb} \leq T_{max}$	25			15			
SVR	Supply voltage rejection ratio ( $R_S = 50\Omega$ ) $T_{amb} = +25^{\circ}C$	80	86		70	86		dB
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
$I_{CC}$	Supply current, no load $T_{amb} = +25^{\circ}C$		1.4	2.5		1.4	2.5	mA
	$T_{min} \leq T_{amb} \leq T_{max}$			2.5		2.5		
$V_{icm}$	Input common mode voltage range	$\pm 11$	+15 -12		$\pm 11$	+15 -12		V
CMR	Common mode rejection ratio ( $R_S = 50\Omega$ ) $T_{amb} = +25^{\circ}C$	80	86		70	86		dB
	$T_{min} \leq T_{amb} \leq T_{max}$	80			70			
$I_{os}$	Output short-circuit current $T_{amb} = +25^{\circ}C$	10	40	60	10	40	60	mA
	$T_{min} \leq T_{amb} \leq T_{max}$	10		60	10		60	
$\pm V_{opp}$	Output voltage swing $T_{amb} = +25^{\circ}C$	$R_L = 2k\Omega$	10	12		10	12	V
		$R_L = 10k\Omega$	12	13.5		12	13.5	
		$T_{min} \leq T_{amb} \leq T_{max}$	10			10		
		$R_L = 10k\Omega$	12			12		
SR	Slew rate $V_{in} = 10V$ , $R_L = 2k\Omega$ , $C_L = 100pF$ , unity gain	8	16		8	16		V/ $\mu s$

Table 3.  $V_{CC} = \pm 15V$ ,  $T_{amb} = +25^{\circ}C$  (unless otherwise specified) (continued)

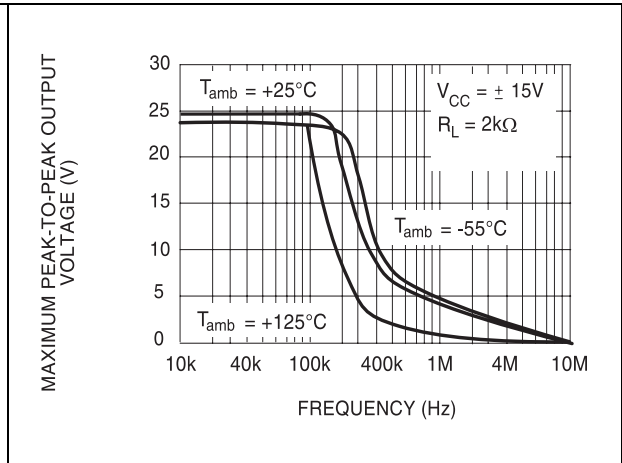
Symbol	Parameter	TL082I,AC,AI,BC, BI			TL082C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_r$	Rise time $V_{in} = 20mV$ , $R_L = 2k\Omega$ , $C_L = 100pF$ , unity gain		0.1			0.1		$\mu s$
$K_{ov}$	Overshoot $V_{in} = 20mV$ , $R_L = 2k\Omega$ , $C_L = 100pF$ , unity gain		10			10		%
GBP	Gain bandwidth product $V_{in} = 10mV$ , $R_L = 2k\Omega$ , $C_L = 100pF$ , $F = 100kHz$	2.5	4		2.5	4		MHz
$R_i$	Input resistance		$10^{12}$			$10^{12}$		$\Omega$
THD	Total harmonic distortion $F = 1kHz$ , $R_L = 2k\Omega$ , $C_L = 100pF$ , $A_v = 20dB$ , $V_o = 2V_{pp}$		0.01			0.01		%
$e_n$	Equivalent input noise voltage $R_S = 100\Omega$ , $F = 1kHz$		15			15		$\frac{nV}{\sqrt{Hz}}$
$\phi_m$	Phase margin		45			45		degrees
$V_{o1}/V_{o2}$	Channel separation $A_v = 100$		120			120		dB

1. The input bias currents are junction leakage currents which approximately double for every  $10^{\circ}C$  increase in the junction temperature.

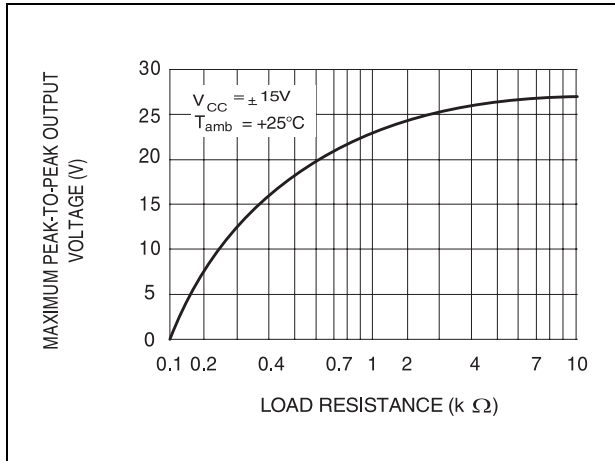
**Figure 2. Maximum peak-to-peak output voltage versus frequency**



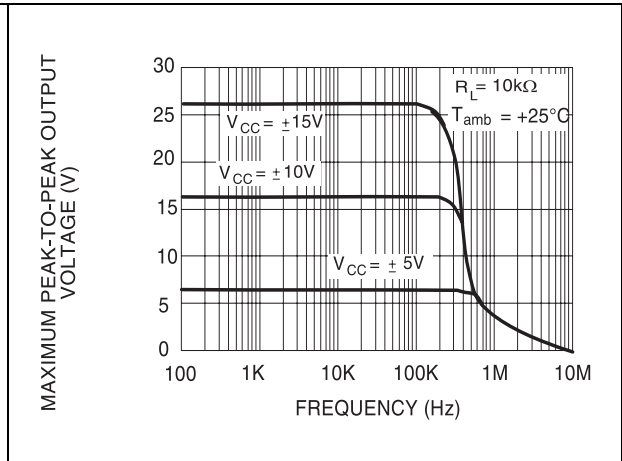
**Figure 3. Maximum peak-to-peak output voltage versus frequency**



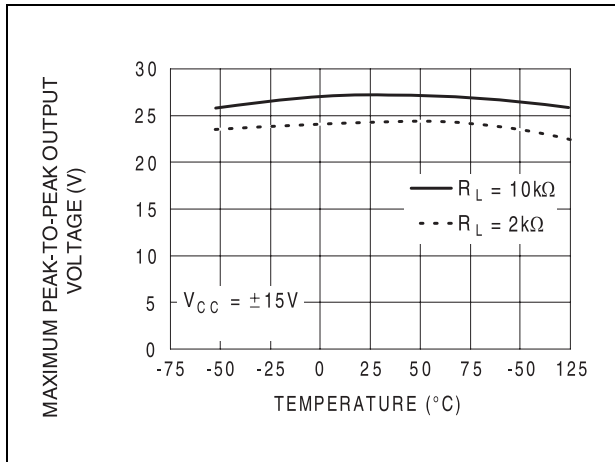
**Figure 4. Maximum peak-to-peak output voltage versus load resistance**



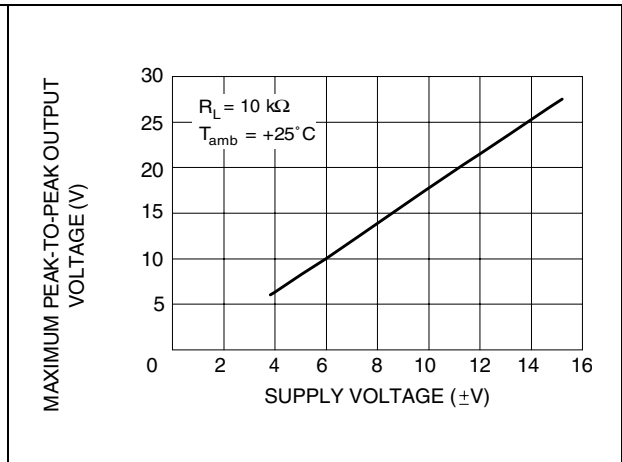
**Figure 5. Maximum peak-to-peak output voltage versus frequency**



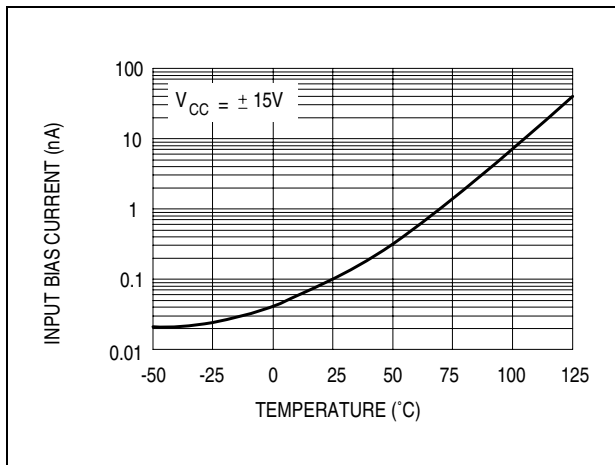
**Figure 6. Maximum peak-to-peak output voltage versus free air temperature**



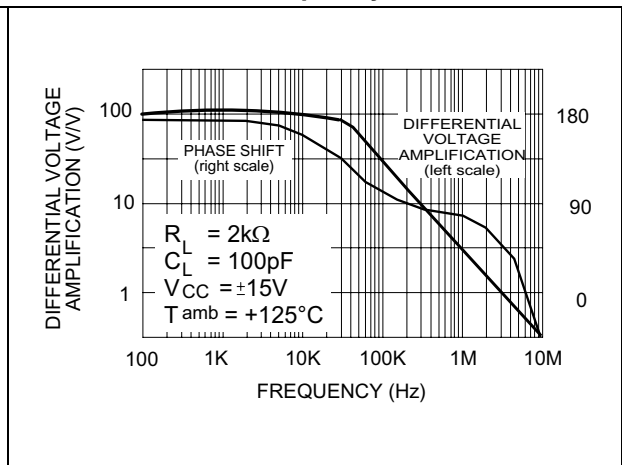
**Figure 7. Maximum peak-to-peak output voltage versus supply voltage**



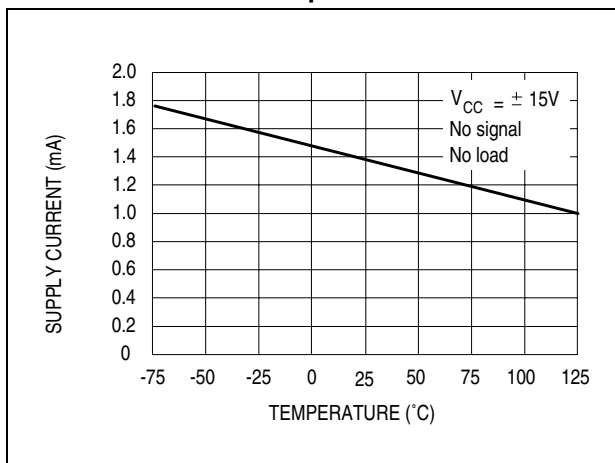
**Figure 8. Input bias current versus free air temperature**



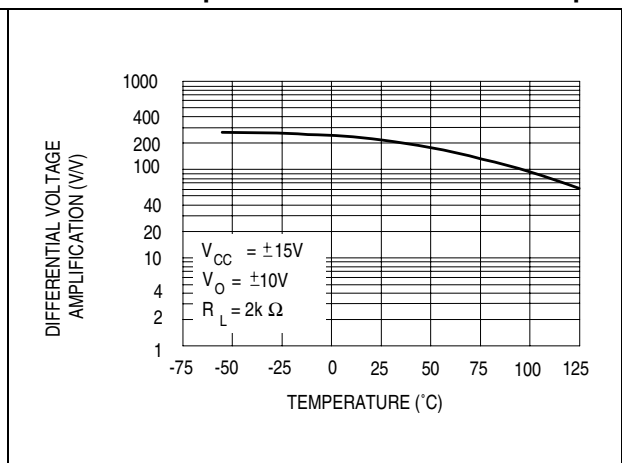
**Figure 9. Large signal differential voltage amplification and phase shift versus frequency**



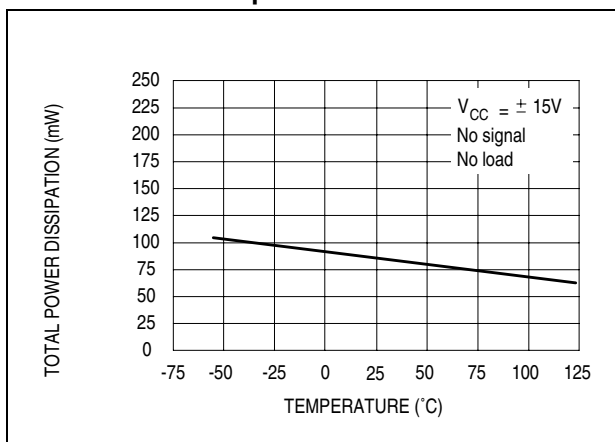
**Figure 10. Supply current per amplifier versus free air temperature**



**Figure 11. Large signal differential voltage amplification versus free air temp.**



**Figure 12. Total power dissipation versus free air temperature**



**Figure 13. Supply current per amplifier versus supply voltage**

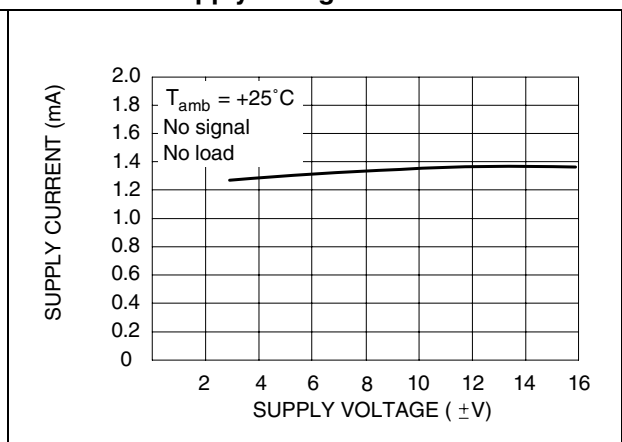


Figure 14. Common mode rejection ratio versus free air temperature

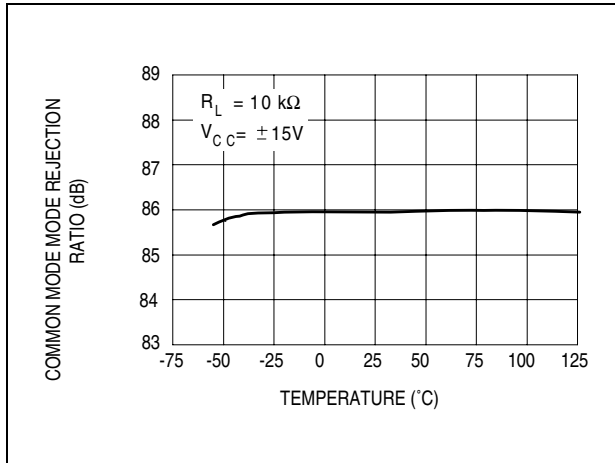


Figure 15. Output voltage versus elapsed time

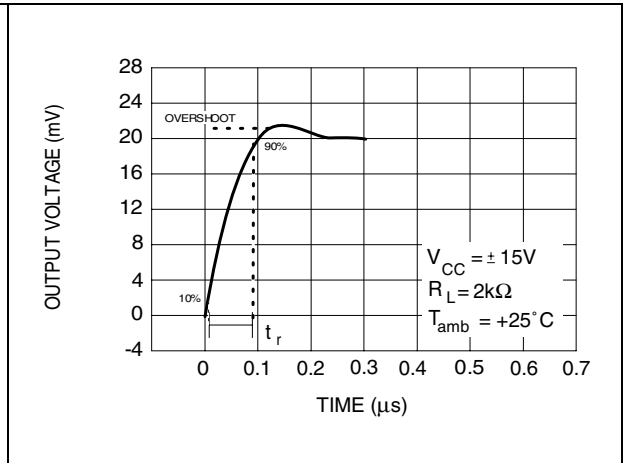


Figure 16. Voltage follower large signal pulse response

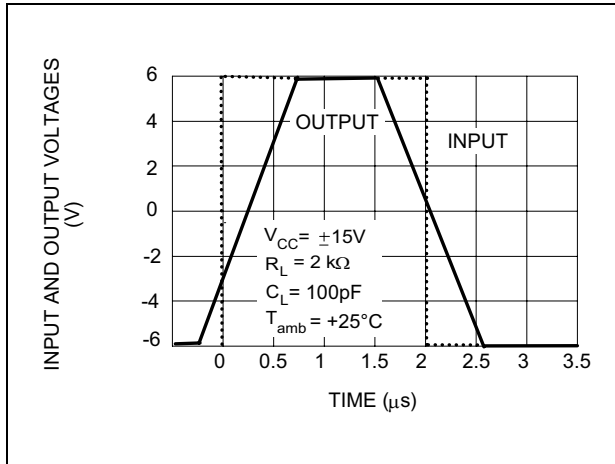


Figure 17. Equivalent input noise voltage versus frequency

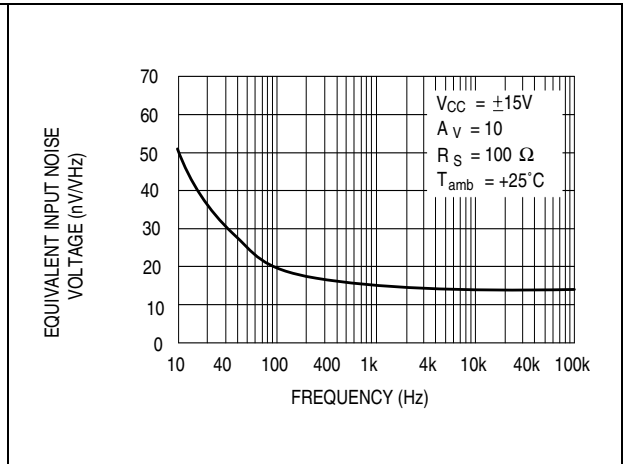
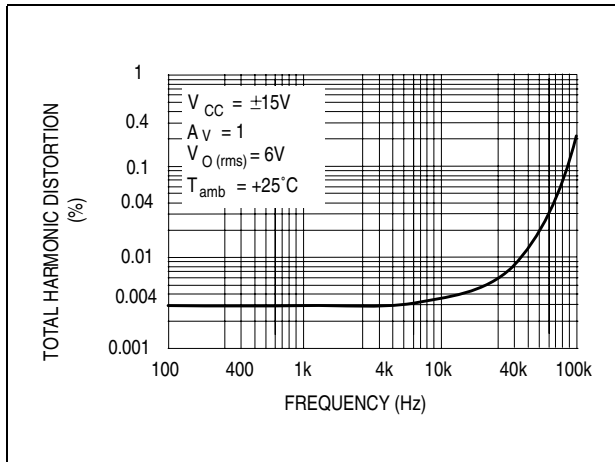


Figure 18. Total harmonic distortion versus frequency





## 4 Parameter measurement information

Figure 19. Voltage follower

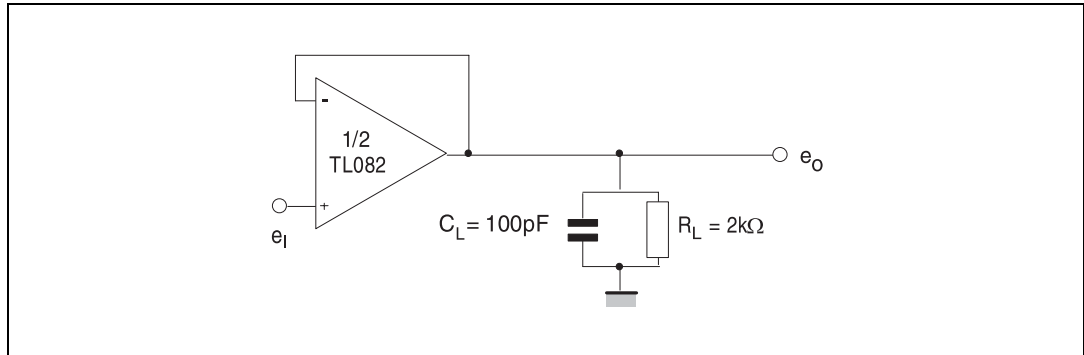
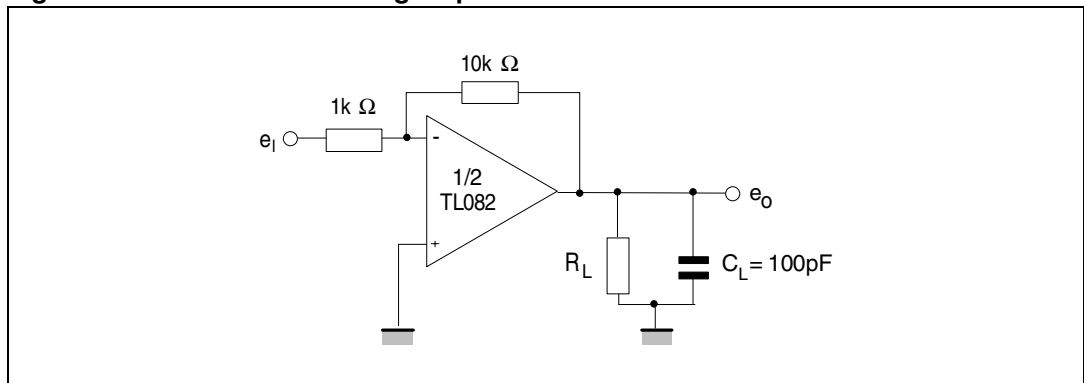
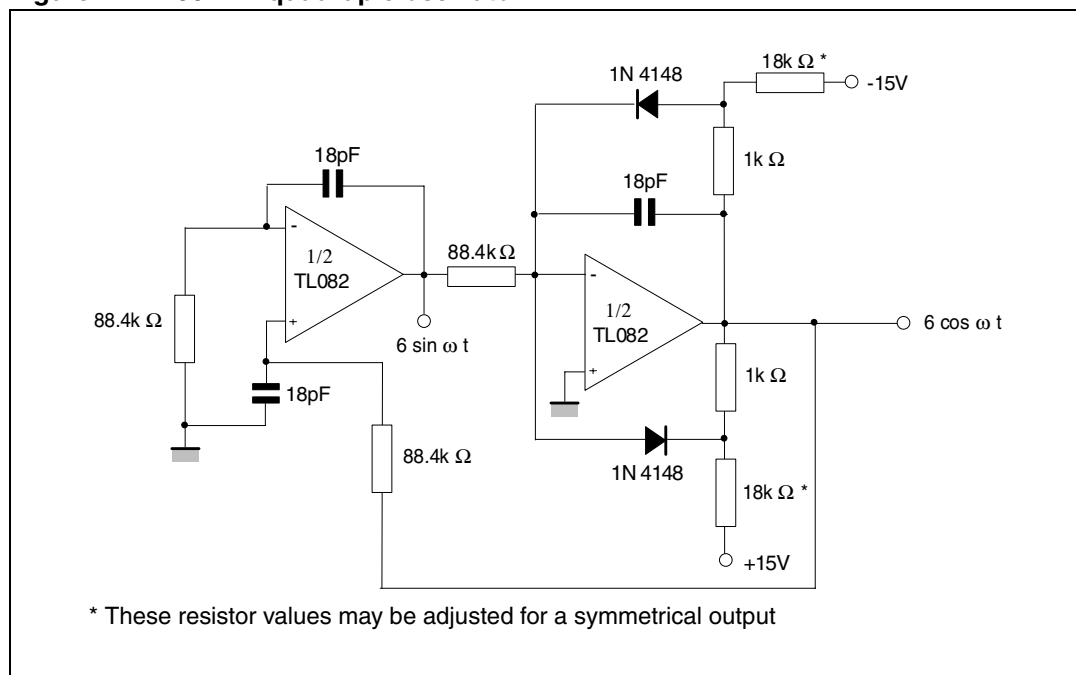


Figure 20. Gain-of-10 inverting amplifier



## 5 Typical applications

Figure 21. 100 kHz quadruple oscillator



## 6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK<sup>®</sup> packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 6.1 DIP8 package information

Figure 22. DIP8 package mechanical drawing

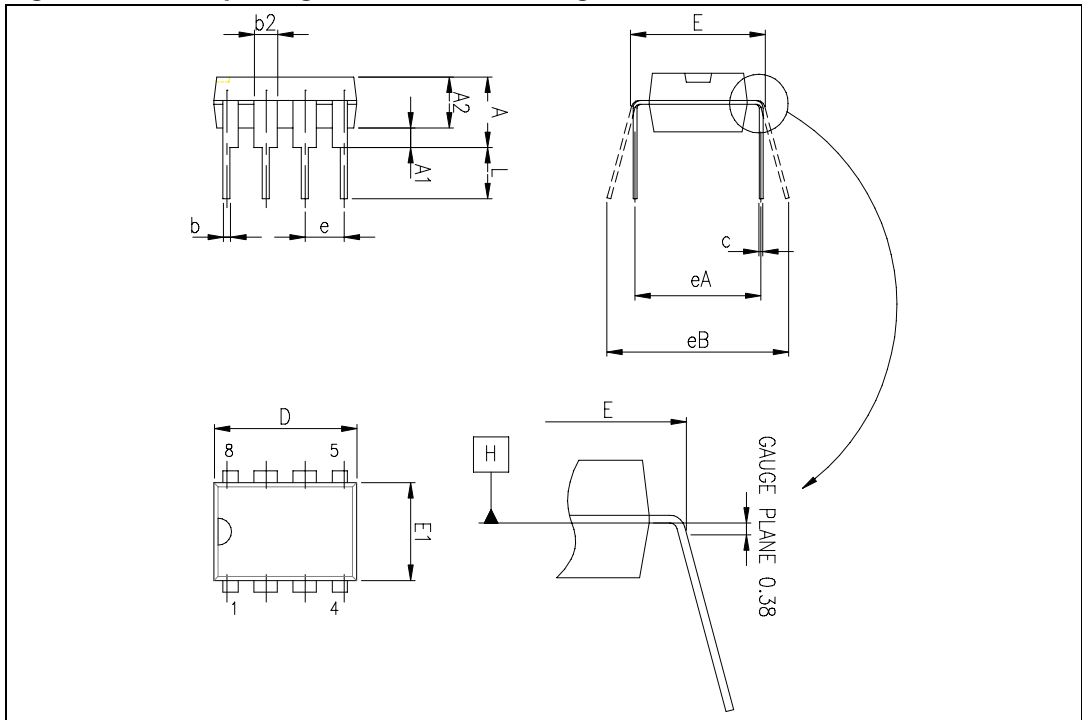


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

## 6.2 SO-8 package information

Figure 23. SO-8 package mechanical drawing

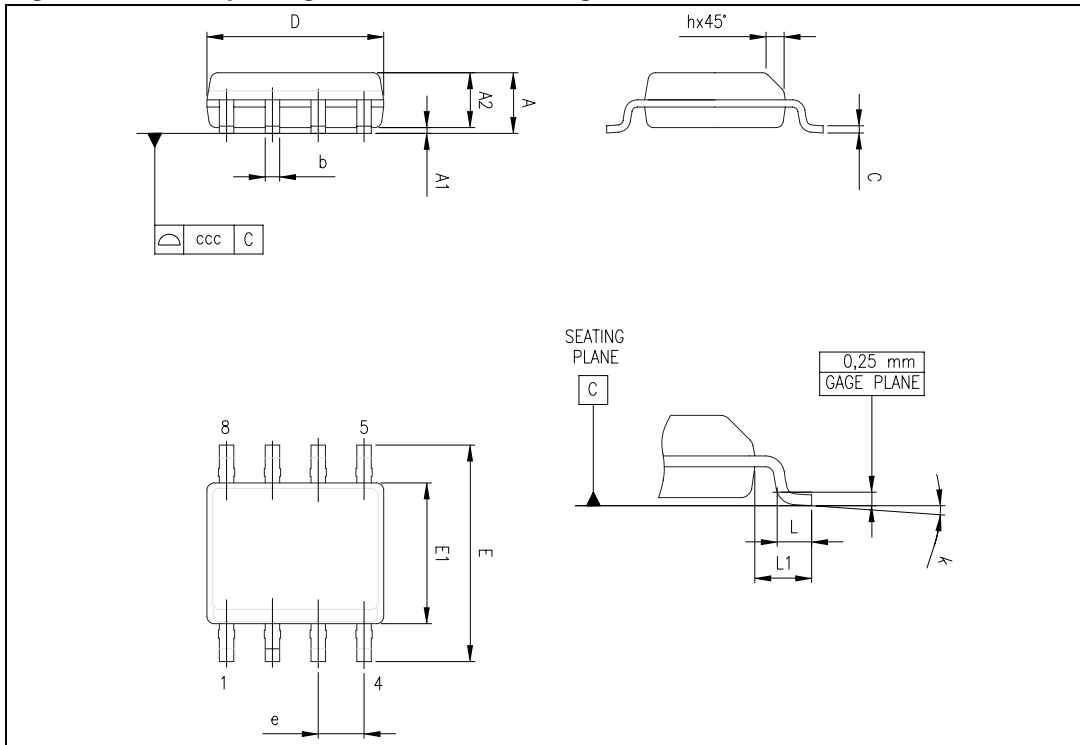


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

### 6.3 TSSOP8 package information

Figure 24. TSSOP8 package mechanical drawing

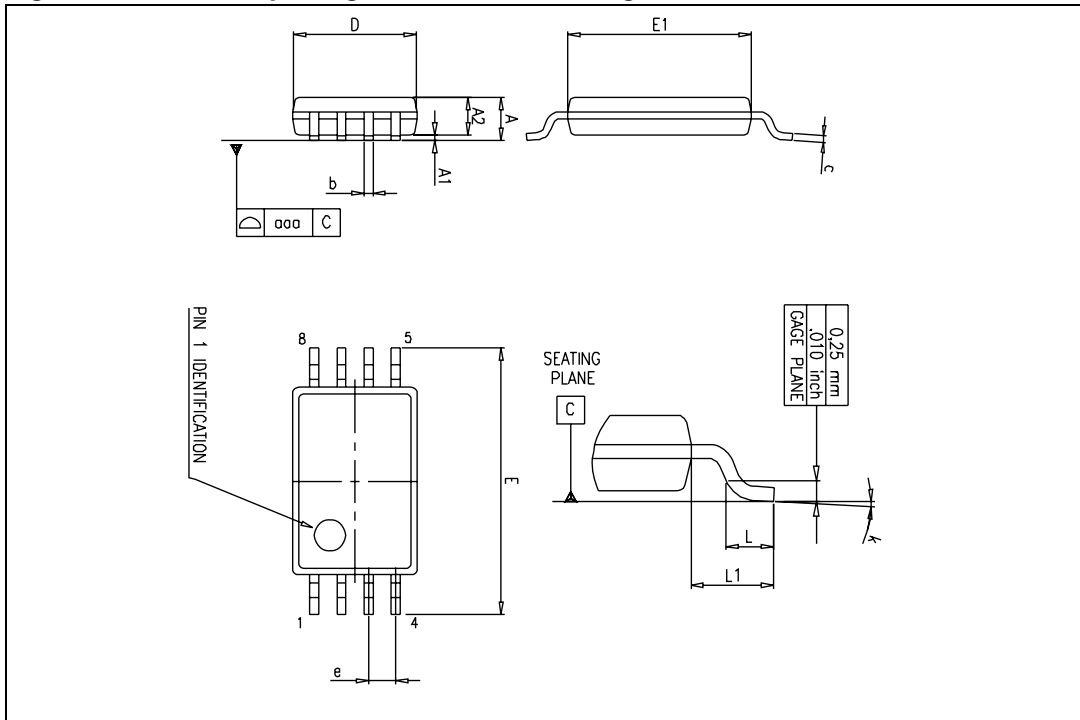


Table 6. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	

# 7 Ordering information

**Table 7. Order codes**

Order code	Temperature range	Package	Packing	Marking
TL082IN	-40°C, +105°C	DIP8	Tube	TL082IN
TL082ID TL082IDT		SO-8	Tube or tape & reel	082I
TL082IPT		TSSOP8	Tape & reel	
TL082AIN		DIP8	Tube	TL082AIN
TL082AID TL082AIDT		SO-8	Tube or tape & reel	082AI
TL082AIPT		TSSOP8	Tape & reel	
TL082BIN		DIP8	Tube	TL082BIN
TL082BID TL082BIDT		SO-8	Tube or tape & reel	082BI
TL082BIPT		TSSOP8	Tape & reel	
TL082CN		0°C, +70°C	DIP8	Tube
TL082CD TL082CDT	SO-8		Tube or tape & reel	082C
TL082CPT	TSSOP8		Tape & reel	
TL082ACN	DIP8		Tube	TL082ACN
TL082ACD TL082ACDT	SO-8		Tube or tape & reel	082AC
TL082ACPT	TSSOP8		Tape & reel	
TL082BCN	DIP8		Tube	TL082BCN
TL082BCD TL082BCDT	SO-8		Tube or tape & reel	082BC
TL082BCPT	TSSOP8		Tape & reel	
TL082IYDT <sup>(1)</sup>	-40°C, +105°C		SO8 (automotive grade)	Tube or tape & reel
TL082AIYDT <sup>(1)</sup>		82AIY		
TL082BIYDT <sup>(1)</sup>		82BIY		

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

## 8 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
02-Apr-2001	1	Initial release.
2002-2003	2-7	Internal revisions.
30-Apr-2004	8	Format update.
06-Mar-2007	9	Added ESD information in <a href="#">Table 1 on page 3</a> . Expanded order codes table and added automotive grade order codes. See <a href="#">Table 7 on page 15</a> . Added <a href="#">Table 2: Operating conditions on page 3</a> . Updated package information to make it compliant with the latest JEDEC standards.
17-Jun-2008	10	Removed information concerning military temperature range (TL082M*, TL082AM*, TL082BM*).



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